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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/753,615	01/08/2004	Stuart W. Hayes	016295.1509 (DC-05592)	6328
23640	7590	11/01/2006	EXAMINER	
BAKER BOTTS, LLP			DINH, TUAN T	
910 LOUISIANA			ART UNIT	
HOUSTON, TX 77002-4995			PAPER NUMBER	

2841

DATE MAILED: 11/01/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

10/753,615

Applicant(s)

HAYES ET AL.

Examiner

Tuan T. Dinh

Art Unit

2841

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 18 August 2006.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 16-31 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 16-31 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |  |   |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892)                     | 4) <input type="checkbox"/> Interview Summary (PTO-413)           |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____                                      |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)          | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date _____  | 6) <input type="checkbox"/> Other: _____                          |

## DETAILED ACTION

### ***Claim Rejections - 35 USC § 112***

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims 21-31 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Regarding claim 21, lines 8-11, and claim 26, lines 6-8 are unclear. The phrase of “an electrically trace not in contact with the voltage and ground...first and second portions lying in first and second plane that reference the voltage planes” is not understood because the trace is distinct from the voltage and ground plane so how can the trace **be referenced** the voltage and ground planes?

By applying art, the examiner assume that the phrase should be read as “the trace having first and second portions lying in first and second planes”

### ***Claim Rejections - 35 USC § 102***

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Art Unit: 2841

4. Claims 21-25 are rejected under 35 U.S.C. 102(b) as being anticipated by Selna (U.S. Patent 5,640,048).

As to claims 21-25, Selna discloses a high -peed circuit capable of being used in an information handling system comprising:

an integrated circuit (12) coupled to circuit board (100), the circuit board comprising: electrically conductive voltage and ground planes (200, 206), see figure 3 forming first and second layers of the circuit board; and

an electrically conductive trace (8, 10) not in electrical contact with the voltage and ground planes, comprising: first and second portions lying in first and second planes; first electrically conductive via (6C) contacting a first point of the first portion and contacting to a first point of the second portion; and a second electrically conductive via (6C) contacting a second point of the first portion and contacting to a second point of the second portion.

As to claim 26-31, Selna discloses a high speed package capable of being used in an information handling system, comprising: an integrated circuit (12) coupled to a circuit board (100), the circuit board comprising: electrically conductive voltage and ground planes; and an electrically conductive trace (8, 10) comprising: first and second portions lying in first and second planes; a first electrically conductive via (6C) contacting a first point of the first portion and contacting the a first point of the second portion; and a second electrically conductive via (6C) contacting a second point of the first portion and contacting a second point of the second portion.

**Claim Rejections - 35 USC § 103**

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claims 16-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Selna (U.S. Patent 5,640,048) in view of Teshome et al. (U.S. Patent 6,236,572).

As to claim 16, Selna discloses a BGA package for IC capable of being used in an information handling system as shown in figure 3 comprising:

a circuit board (100) having an electrical trace (8, 10, the elements 8 and 10 formed on to and bottom surfaces of the board 100)) and voltage and ground planes (260, 200, column 7, lines 56-59) formed on first and second layers, the electrical trace (8, 10, see figure 3) routed over a portion of the circuit board and electrically distinct from the voltage and ground plane,

the electrical trace (8, 10) including first and second paths (8C, 10C) such that the first path references the ground plane and the second path references the voltage plane whereby the first path is substantially similar to the second path; and the first path electrically coupled to the second path proximate to at each of the ends of the paths (the electrical connection of the first and second paths defined by conductors filled in Vss vias 6C).

Selna does not disclose the circuit board (100) having a processor and a memory chip communicatively coupled to.

Teshome et al. teaches a computer system as shown in figures 1-2 comprising a memory (24, 26) communicatively coupled to a processor (12), and communicatively coupled to a printed multilayer circuit board (28). It would have been obvious to one having ordinary skill in the art at the time the invention was made to have a teaching of Teshome employed in the package of Selna in order to storing data, and facilitate and control data signals for the computer.

As to claim 17, Selna discloses the first path (8C) is located at a distance from the ground plane (200) that is substantially equal to the distance the second path (10C) is located from the voltage plane (260).

As to claim 18, Selna discloses the ground and voltage planes (200, 260) are symmetrically oriented about the circuit board.

As to claim 19, Selna discloses the first and second paths (8C, 10C) and the second path are symmetrically oriented about the circuit board.

As to claim 20, Selna discloses in figure 3 the first path and the ground plane are a mirror image of the second path and the voltage plane.

### ***Response to Arguments***

Applicant's arguments with respect to claims 16-31 have been considered but are moot in view of the new ground(s) of rejection.

Applicant argues:


Selna does not disclose the trace electrically distinct from the voltage and ground planes. Examiner disagrees because as shown in figure 3 that the trace (8, 10) are distinct from the voltage or the ground planes by insulating layers (272, 282).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tuan T. Dinh whose telephone number is 571-272-1929. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Enad Elvin can be reached on 571-272-1990. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Tuan Dinh  
October 25, 2006.

  
10/25/06  
Tuan Dinh.